Docket No.: SON-2047
(80001-2047)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Akihiko KOH et al.

Confirmation No.: 3304

Application No.: 09/802,857

Art Unit: 2122

Filed: March 12, 2001

Examiner: M. J. Yigdall

For: DATA PROCESSING APPARATUS PERFORMING PREDETERMINED DATA PROCESSING IN ACCORDANCE WITH INSTRUCTION CODES READ FROM A PROGRAM MEMORY STORING A PROGRAM (as amended)

REPLY BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

INTRODUCTORY COMMENTS

This is a Reply Brief under 37 C.F.R. §41.41 in response to the Examiner's Answer mailed on August 9, 2005.

All arguments presented within the Appeal Brief of April 22, 2005 are incorporated herein by reference. Additional arguments are provided hereinbelow.

Claims 13-25 are currently pending and finally rejected in this application, with claim 13 being independent. For purposes of the issues presented by this appeal:

Claims 13-18 and 21-25 stand or fall together.

Claim 19 stands or falls alone.

Claim 20 stands or falls alone.

As an initial matter, paragraph 9 of the Examiner's Answer contends to include a response to the arguments made within the Appeal Brief.

In response to the contentions made within paragraph 9 of the Examiner's Answer, please note that these contentions, even if true, fail to rebut the arguments set forth within the Appeal Brief.

Claims 13-18 and 21-25 - Claim 13 is drawn to a data processing apparatus performing predetermined data processing in accordance with instruction codes read from a program memory storing a program, the data processing apparatus comprising:

> a debugging circuit having a plurality of bug address setting registers and a plurality of coincidence detecting circuits,
>
> one of said plurality of bug address setting registers holding one of a plurality of bug addresses that show the start of a buggy part of said program stored in said program memory,
>
> one of said plurality of coincidence detecting circuits comparing a program address for reading instruction codes from said program memory with said one of said plurality of bug addresses held in said one of said plurality of bug address setting registers, said one of said plurality of coincidence detecting circuits outputting one of a plurality of coincidence signals when said program address and said one of said plurality of bug addresses coincide,

another of said plurality of bug address setting registers holding another of said plurality of bug addresses that show the start of another buggy part of the program stored in the program memory,

another of said plurality of coincidence detecting circuits comparing said program address for reading instruction codes from said program memory with said another of said plurality of bug addresses held in said another of said plurality of bug address setting registers, said another of said plurality of coincidence detecting circuits outputting another of said plurality of coincidence signals when said program address and said another of said plurality of bug addresses coincide; and

a central processing unit receiving said plurality of coincidence signals, wherein said central processing unit:

executes one of a plurality of debugging programs stored within random access memory when said one of said plurality of coincidence signals indicates a coincidence of said program address and said one of said plurality of bug addresses,

executes another of said plurality of debugging programs stored within said random access memory when said another of said plurality of coincidence signals indicates a coincidence of said program address and said another of said plurality of bug addresses, and

executes said program stored within said program memory when said plurality of coincidence signals indicates a non-coincidence of said program address and any of said plurality of bug addresses.

The Examiner's Answer notes that Figure 1 of U.S. Patent No. 5,454,100 to Sagane arguably teaches **a** coincidence signal E (Examiner's Answer at page 4). In this regard, the Examiner's Answer fails to show where within Figure 1 of Sagane is to be found **a plurality of** coincidence signal**s** E.

Sagane arguably teaches that in Figures 3 and 1, like reference characters designate like or corresponding parts, and repetitive descriptions of the parts in Figure 3 are omitted (Sagane at column 6, lines 2-6).

The first embodiment of Sagane arguably depicts a comparator 8 that supplies the *interrupt control circuit 7d* with an interrupt (Sagane at Figure 1, column 5, lines 13-17).

Sagane arguably teaches that another modification of the second embodiment is to interpose the control flag switch 7a and switch 7c of Figure 1 between the comparator 8 and the *switch 23* in Figure 3 (Sagane at column 7, lines 3-6).

However, nowhere within Sagane is there found a disclosure, teaching or suggestion that the *interrupt control circuit 7d* of Figure 1 corresponds with the *switch 23* of Figure 3. Whereas Figure 1 arguably depicts a link between the interrupt control circuit 7d and the CPU 2, no such link is found within Figure 3 of Sagane between the switch 23 and the CPU 2.

Regarding Figure 3 of Sagane, the Examiner's Answer contends that a plurality of comparators 8 is provided to address multiple bugs, and each comparator 8 outputs a coincidence signal (Examiner's Answer at page 5).

In response to this contention, the second embodiment of Sagane fails to expressly state that each of the pluralities of comparators 8 described at column 7, line 1 of Sagane would necessarily output a coincidence signal. But even if each of the pluralities of comparators 8 described at column 7, line 1 of Sagane would necessarily output a coincidence signal, the Examiner's Amendment *fails to clearly identify* within the second embodiment of Sagane *where and how the CPU 2 is to receive a plurality of coincidence signals*, since signal A of comparator 8 found within Figure 3 is applied to switch 23 and ***not to the CPU 2.*** Thus, all claimed features are absent from within the second embodiment of Sagane.

The Examiner's Answer contends that *Appellant does not dispute that the match circuits of U.S. Patent No. 5,701,506 to Hosotani are analogous to the comparators of Sagane and that both*

are equated with the "coincidence detecting circuits" recited in claim 13 (Examiner's Answer at page 5).

In response to this contention, the Appeal Brief has disputed the teaching of Hosotani in relation to Sagane and claim 13. In particular, pages 11-12 of the Appeal Brief provide that:

> The Office Action cites Hosotani for the features deficient within Sagane. Hosotani arguably teaches microcomputer having ROM program that can be altered. Within Hosotani the first to third match circuits 9a-9c are connected to a three-input OR circuit 14. Hosotani arguably teaches that the output of OR circuit 14 is applied to switch 10 (Hosotani at Figures 2, 6, 8, 10, 11) or to ROM 17 (Hosotani at Figures 7, 12). Yet, Hosotani fails to disclose, teach or suggest the output of OR circuit 14 being applied to CPU 1. *Thus, Hosotani fails to disclose, teach, or suggest a central processing unit receiving a plurality of coincidence signals.* (Emphasis added).

However, the Examiner's Answer contends that the output of the comparator 8 determines *which **data** the CPU 2 receives* (Examiner's Answer at page 5). Nevertheless, even if this is true, the Examiner's Answer fails to show that that *data* that the CPU 2 receives within Figure 2 of Sagane are the alleged coincidence signals A from the comparator 8.

The Examiner's Answer contends that switch 23 found within Figure 3 of Sagane is the mechanism by which the CPU 2 "receives" *the effect of* the coincidence signal A from the comparator 8 (Examiner's Answer at page 6).

The Examiner's Answer further contends that the plain language of the claim does not include and/or exclude any such direct or indirect means for "receiving" (Examiner's Answer at page 6).

In response, the Examiner's Answer has failed to show that the CPU 2 as allegedly *receiving the effect of the coincidence signal A* is, in fact, the CPU 2 as *receiving the coincidence signal A* itself. In this regard, there is no teaching within Figure 3 of the alleged coincidence signal A being received by the CPU 2.

The Examiner's Answer contends that Sagane teaches a plurality of start addresses stored within the interrupt vector register 7b (Examiner's Answer at page 8).

In response to this contention, while interrupt vector register 7b of Sagane is found within Figure 1 of Sagane, interrupt vector register 7b is *absent* from within Figure 3 of Sagane. As shown hereinabove and within the Appeal Brief, a plurality of coincidence signals is not to be found within Figure 1 of Sagane. Thus, Sagane fails to disclose, teach or suggest the execution of a debugging program when ***one of the coincidence signals*** indicates a coincidence of the program address and the one of the plurality of bug addresses, along with the execution of another debugging program when ***another of the coincidence signals*** indicates a coincidence of the program address and the another of the plurality of bug addresses.

The Examiner's Answer contends that switching unit 7 in Figure 1 of Sagane and switch 23 in Figure 3 of Sagane are analogous (Examiner's Answer at page 9).

Nevertheless, regarding the switching unit 7 in Figure 1 of Sagane, the coincidence signal E of Figure 1 enters an interrupt control circuit 7d as an interrupt request signal (Sagane at column 3, lines 59-60). If the two addresses coincide with each other, the comparator 8 supplies the interrupt control circuit 7d with a coincidence signal E via the switch 7c, thereby *generating an interrupt* in step S8 of Sagane (Sagane at Figure 2, column 5, lines 13-17). However, the switch 23 in Figure 3 of Sagane fails to generate an interrupt in step 28 (Sagane at Figure 4). Thus, Examiner's Answer has *failed* to show that that switching unit 7 in Figure 1 of Sagane and switch 23 in Figure 3 of Sagane are analogous.

The Examiner's Answer contends that the switch or connection control means 10 is a mechanism by which the CPU 1 of Hosotani "receives" the effect of the plurality of coincidence signals from the match circuits 9a-9c (Examiner's Answer at page 10).

In response, the Examiner's Answer has failed to show that the CPU 1 allegedly *receiving the effect of the* plurality of coincidence signals from the match circuits 9a-9c is, in fact, the CPU 1 as *receiving the* plurality of coincidence signals from the match circuits 9a-9c

themselves. In this regard, there is no teaching within Hosotani of the alleged plurality of coincidence signals from the match circuits 9a-9c being received by the CPU 1.

Claim 19 - Claim 19 is drawn to a data processing apparatus as set forth in claim 13, wherein said central processing unit receives said plurality of coincidence signals as separate interrupt requests.

Within claim 19, the central processing unit receives the plurality of coincidence signals as separate interrupt requests.

The Examiner's Answer cites Sagane at column 5, lines 13-16 and 49-54, for this teaching (Examiner's Answer at page 11). However, these passages within Sagane refer only to the first embodiment of Sagane. The first embodiment of Sagane fails to disclose, teach, or suggest a plurality of coincidence signals.

Claim 20 - Claim 20 is drawn to a data processing apparatus as set forth in claim 13, wherein said central processing unit receives said plurality of coincidence signals as a single interrupt request.

Within claim 20, the central processing unit receives the plurality of coincidence signals as a single interrupt request.

The Examiner's Answer cites Hosotani for this teaching (Examiner's Answer at page 11). However, a review of Figure 2 of Hosotani reveals that a signal from OR gate 14, while being s received by a switch 10, is not received by the CPU 1.

Conclusion

The prior art of record, either individually or as a whole, fails to disclose, teach, or suggest all the features of the claimed invention. For at least the reasons set forth hereinabove, the rejection of the claimed invention should not be sustained.

Therefore, a reversal of the rejection of November 19, 2004 is respectfully requested.

If any fee is required or any overpayment made, the Commissioner is hereby authorized to charge the fee or credit the overpayment to Deposit Account # 18-0013.

Dated: October 11, 2005

Respectfully submitted,

By_____

Ronald P. Kananen
Registration No.: 24,104
RADER, FISHMAN & GRAUER PLLC
1233 20th Street, N.W.
Suite 501
Washington, DC 20036
(202) 955-3750
Attorney for Applicant